UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,004	02/08/2002	Woo Young So	1514.1010	6442

49455 7590 01/16/2008

STEIN, MCEWEN & BUI, LLP
1400 EYE STREET, NW
SUITE 300
WASHINGTON, DC 20005

EXAMINER	
SEFER, AHMED N	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
01/16/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/068,004	SO ET AL.	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12,14-16,22 and 24-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *12,14-16,22 and 24-38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/31/2007 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 12, 14-16, 26 and 28-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura et al. ("Takemura") USPN 5,962,897 in view of Yamazaki et al. USPN 6,617,648 ("Yamazaki '648").

Takemura discloses in figs. 5 and 6 a thin film transistor (TFT), comprising: a substrate 11; a semiconductor layer 13 formed over said substrate having end portions; a first insulating layer 14 disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer (figs. 5D and 6D); a gate electrode 15 formed over said first insulating layer; a capping layer 16 formed over said gate electrode; spacers 22 formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer; high-

density source and drain regions (17, 19) formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer; and source and drain electrodes (29, 30) which respectively contact said high-density source and drain regions without contact holes, but does not disclose low-density source and drain regions under said spacers.

Yamazaki '648 discloses in fig. 6 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate having end portions; low-density source and drain regions 611 having a same conductivity as high-density source and drain regions (609, 610) formed at regions of said semiconductor layer under spacers 608 between the gate electrode 604 and the high density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions under said spacers.

Therefore, in view of Yamazaki '648, one having ordinary skill in the art at the time the invention was made would be motivated to modify Takemura by incorporating lightly doped drain (LDD) regions under said spacers. The motivation would be to minimize kink effect. Therefore, it would have been obvious to combine Takemura and Yamazaki '648 so as to yield the device of claim 12.

Re claim 14, Takemura discloses (col. 16, lines 13 and 56 and col. 17, line 19) said first insulating layer, said capping layer and said spacer are of an oxide.

Re claims 15 and 16, Yamazaki '648 discloses in fig. 7 a silicide layer being formed between said source electrode and said high density source region and a silicide 704 between said drain electrode and said high density drain region; wherein said silicide layer comprise refractory metal **(as recited in claim 16)**.

Re claim 26, Yamazaki '648 discloses said high-density source and drain regions and said low-density source and drain regions extend through an entire thickness of said semiconductor layer.

Re claim 28, Yamazaki '648 discloses said high-density source and drain regions being formed at entireties of the end portions of said semiconductor layer exposed beyond said spacers; and wherein said low-density source and drain regions having a same conductivity as said high-density source and drain regions are formed at entireties of regions of semiconductor layer entirely under said spacers between the gate electrode and the high-density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers.

Re claim 29, Takemura discloses source and drain electrodes (29, 30) that do not contact high-density source and drain regions (17, 19) via any electrode material filling any contact holes.

Re claim 30, Takemura discloses the capping layer 16 and the spacers 22 being separate layers.

Re claim 31, Yamazaki '892 discloses source and drain electrodes (614, 615) that do not contact a capping layer 605; and wherein the source and drain electrodes do not contact the spacers 608.

4. Claims 12, 26, 28-31 35 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura in view of Ohtani et al. ("Ohtani") US PG-Pub 2007/0210451.

Takemura discloses in figs. 5 and 6 a thin film transistor (TFT), comprising: a substrate 11; a semiconductor layer 13 formed over said substrate having end portions; a first insulating

layer 14 disposed on said semiconductor layer so as to expose ones of the end portions of said semiconductor layer (figs. 5D and 6D); a gate electrode 15 formed over said first insulating layer; a capping layer 16 formed over said gate electrode; spacers 22 formed over said first insulating layer and on both sidewall portions of said gate electrode and said capping layer; high-density source and drain regions (17, 19) formed at the ones of the end portions of said semiconductor layer exposed beyond said spacers, the high-density source and drain regions spaced apart from the gate electrode and the capping layer; and source and drain electrodes (29, 30) which respectively contact said high-density source and drain regions without contact holes, but does not disclose low-density source and drain regions under said spacers.

Ohtani discloses in fig. 4 a thin film transistor (TFT), comprising: a substrate; a semiconductor layer formed over said substrate having end portions (fig. 4B); low-density source and drain regions 66 having a same conductivity as high-density source and drain regions (69, 70) formed at regions of said semiconductor layer under spacers 88 (fig. 4B) between the gate electrode 64 and the high density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions under said spacers.

Therefore, in view of Ohtani, one having ordinary skill in the art at the time the invention was made would be motivated to modify Takemura by incorporating lightly doped drain (LDD) regions under said spacers. The motivation would be to minimize kink effect. Therefore, it would have been obvious to combine Takemura and Ohtani so as to yield the device of claim 12.

Re claim 26, Ohtani discloses said high-density source and drain regions and said low-density source and drain regions extend through an entire thickness of said semiconductor layer.

Re claim 28, Ohtani discloses said high-density source and drain regions being formed at entireties of the end portions of said semiconductor layer exposed beyond said spacers; and wherein said low-density source and drain regions having a same conductivity as said high-density source and drain regions are formed at entireties of regions of semiconductor layer entirely under said spacers between the gate electrode and the high-density source and drain regions, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers.

Re claim 29, Takemura/Ohtani discloses source and drain electrodes that do not contact high-density source and drain regions via any electrode material filling any contact holes.

Re claim 30, Takemura discloses the capping layer 16 and the spacers 22 being separate layers.

Re claim 31, Ohtani discloses in fig. 8 source and drain electrodes (14a, 114b) that do not contact a capping layer (unnumbered horizontal region covering gates 104 and 105); and wherein the source and drain electrodes do not contact the spacers (unnumbered vertical region on the sidewall of gates 104 and 105).

Re claim 35, Ohtani discloses the source and drain electrodes (14a, 114b) do not contact the high density source drain regions via any electrode material filling any contact holes; the source and drain electrodes (14a, 114b) do not contact the capping layer; and the source and drain electrodes (14a, 114b) do not contact the spacers.

Re claim 36, Takemura discloses the capping layer and the spacer being separate layers.

5. Claims 22, 24, 27, 32-34, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura in view of Ohtani.

Takemura discloses in figs. 5 and 6 an active matrix display device, comprising: a substrate; a semiconductor layer 13 having end portions formed over said substrate; a first insulating layer 14 formed over said semiconductor layer so as to expose end portions of said semiconductor layer; a gate electrode 15 formed over said first insulating layer; a capping layer 16 formed over said gate electrode; spacers 22 formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer; high-density source and drain regions (17, 19) formed at entireties of the end portions of said semiconductor layer exposed beyond said spacers; source and drain electrodes (29, 30) which respectively contact said high density source and drain regions, but does not disclose a low-density source and drain regions and a pixel electrode formed on a planarization layer having an opening portion which exposes a portion of one of said source and drain electrodes.

Ohtani discloses in fig. 4 an active matrix display device, comprising: a substrate; a semiconductor layer having end portions (fig. 4a) formed over said substrate; low-density source and drain regions 66 having a same conductivity as a high-density source and drain regions (69, 70) formed at entireties of off-set regions of said semiconductor layer entirely under spacers 68, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers; a planarization layer 73 having an opening portion which exposes a portion of one of source and drain electrodes (76a, 76b); and a pixel electrode 79 formed on the planarization layer, the pixel electrode contacting the portion of one of the source and drain electrodes through the opening portion.

Therefore, in view of Ohtani, one having ordinary skill in the art at the time the invention was made would be motivated to modify Teramoto's device by incorporating lightly doped drain

(LDD) regions under said spacers. The motivation would be to minimize kink effect. Therefore, it would have been obvious to combine Takemura and Ohtani so as to yield the device of claim 22.

Regarding claim 32, Takemura/Ohtani discloses source and drain electrodes that do not contact high-density source and drain regions via any electrode material filling any contact holes.

Regarding claim 33, Takemura discloses the capping layer 16 and the spacers 22 being separate layers.

Regarding claim 34, Ohtani discloses in fig. 8 source and drain electrodes (114a, 114b) that do not contact a capping layer (unnumbered horizontal region on the sidewall of gates 104 and 105); and wherein the source and drain electrodes do not contact the spacers (unnumbered vertical region on the sidewall of gates 104 and 105).

Re claim 37, Ohtani discloses in fig. 8 the source and drain electrodes (14a, 114b) do not contact high density source drain regions (106, 107) via any electrode material filling any contact holes; the source and drain electrodes (14a, 114b) do not contact the capping layer (unnumbered horizontal region on the sidewall of gates 104 and 105); and the source and drain electrodes (14a, 114b) do not contact the spacers (unnumbered vertical region on the sidewall of gates 104 and 105).

Re claim 36, Takemura discloses the capping layer and the spacer being separate

6. Claims 22, 24, 27 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura in view of Yamazaki '648.

Takemura discloses in figs. 5 and 6 an active matrix display device, comprising: a substrate; a semiconductor layer 13 having end portions formed over said substrate; a first

insulating layer 14 formed over said semiconductor layer so as to expose end portions of said semiconductor layer; a gate electrode 15 formed over said first insulating layer; a capping layer 16 formed over said gate electrode; spacers 22 formed over said first insulating layer and on side wall portions of said gate electrode and said capping layer; high-density source and drain regions (17, 19) formed at entireties of the end portions of said semiconductor layer exposed beyond said spacers; source and drain electrodes (29, 30) which respectively contact said high density source and drain regions, but does not disclose a low-density source and drain regions and a pixel electrode formed on a planarization layer having an opening portion which exposes a portion of one of said source and drain electrodes.

Yamazaki '648 discloses in fig. 6 an active matrix display device, comprising: a substrate; a semiconductor layer 602 having end portions formed over said substrate; low-density source and drain regions 611 having a same conductivity as a high-density source and drain regions (609, 610) formed at entireties of off-set regions of said semiconductor layer entirely under spacers 608, thereby providing said semiconductor layer with lightly doped drain (LDD) regions entirely under said spacers; a planarization layer 349 having an opening portion which exposes a portion of one of said source and drain electrodes; and a pixel electrode 350 formed on the planarization layer, the pixel electrode contacting the portion of one of the source and drain electrodes through the opening portion.

Therefore, in view of Yamazaki '648, one having ordinary skill in the art at the time the invention was made would be motivated to modify Teramoto's device by incorporating lightly doped drain (LDD) regions under said spacers. The motivation would be to minimize kink effect.

Therefore, it would have been obvious to combine Takemura and Yamazaki '648 so as to yield the device of claim 22.

Re claim 24, Yamazaki '648 discloses a silicide layer 704 being formed between a source electrode and said high density source region and a silicide 704 between a drain electrode and said high density drain region

Re claim 27, Yamazaki '648 discloses said high-density source and drain regions and said low-density source and drain regions extend through an entire thickness of said semiconductor layer.

Re claim 32, Takemura discloses source and drain electrodes (29, 30) that do not contact high-density source and drain regions (17, 19) via any electrode material filling any contact holes.

Re claim 33, Takemura discloses the capping layer 16 and the spacers 22 being separate layers.

Re claim 34, Yamazaki '648 discloses source and drain electrodes (614, 615) that do not contact a capping layer 605; and wherein the source and drain electrodes do not contact the spacers 608.

7. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takemura in view of Yamazaki '648 as applied to claim 22 above, and further in view of Yamazaki et al. US PG-Pub 2003/0207502 ("Yamazaki '502").

The combined references disclose an electro-optical device (see Yamazaki '648 col. 1, lines 17-24) but do not specifically disclose an EL layer.

Yamazaki '502 discloses (par. 0343 and fig. 25) an organic electro-luminescence (EL) layer 4029 and a cathode electrode 4030 sequentially formed on a first predetermined area of a pixel electrode and on a second predetermined area of a planarization layer 4142.

Therefore, it would have been obvious to one skilled in the art at the time the invention was made to incorporate an EL layer so as to a realize a high efficiency integrated device which would not need back lights employed in the conventional LCD devices.

Response to Arguments

Applicant's arguments filed 10/31/2007 have been fully considered but they are not persuasive. See Office Action mailed 11/7/2007.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on (571) 272-1236.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

ANS
January 11, 2008

/A. Sefer/
Primary Examiner
Art Unit 2826